

Application Note - Advanced Debugging on the 68HC12

There are two very important issues to consider when implementing the standard 6-way BDM connection for 68HC12 development:-

1. There is no means of controlling the 68HC12's operating mode following a processor reset
2. Communications between target and BDM hardware are restricted to asynchronous

68HC12 Operating Mode

It is important that the 68HC12 device under development is brought out of reset in 'special single chip' mode. If 'special single chip' mode is not entered after reset the 68HC12 begins normal execution and continues to execute until brought under control by entering BDM mode. Since the target is under development it is very likely that the code space will be uninitialised and the processor will therefore not survive real-time execution. Controlling the processor's start-up mode allows code to be downloaded to target memory before the 68HC12 starts execution.

A solution to the problem is to provide the BDM hardware with a means of controlling the initial operating mode of the target system. This can be done using the target's MODA and MODB signals.

Making these signals available to the BDM hardware allows the debugger to control the 68HC12's operating mode following reset. Having gained control of the processor, the flex can configure the desired operating mode and download program code into target memory. All this is achieved before the processor starts execution.

Asynchronous Communications

Asynchronous communications create problems for the developer when the target system changes its CPU clock speed. This is because each time the target clock speed changes a new BDM baud rate must be configured. Without this reconfiguration, the supply of debug information to the debugger collapses.

A solution to the problem is to provide synchronous communication support for the BDM hardware. This requires a suitable signal from the target, fortunately there is such a signal, ECLK. ECLK can be used to synchronise communications in any target where ECLK represents the CPU clock.

By simply making the ECLK signal available on the target it is possible to attach a flying lead from the BDM hardware and communications can then become synchronous.

Adding support for synchronous communications significantly improves the debug environment because changes in target clock speed can be detected and communication baud rates automatically adjusted by the debugger. This is very important if your target dynamically changes the clock speed, for example it slows the clock for power saving.

Unfortunately there are conditions under which the ECLK signal may not be representative of the CPU clock:-

- ECLK is used as an I/O signal
- Accesses to devices with wait states

- Misaligned word accesses at external locations
- Under these conditions ECLK cannot be considered to be a true representation of the CPU clock and synchronous communications cannot be supported. This means dynamic CPU clock switching must be disabled during debug.

Synchronous communications simplify 'hot insertion' (i.e. connection of BDM hardware during target execution) because the hardware automatically senses the BDM baud rate.

Target Design - Recommendations

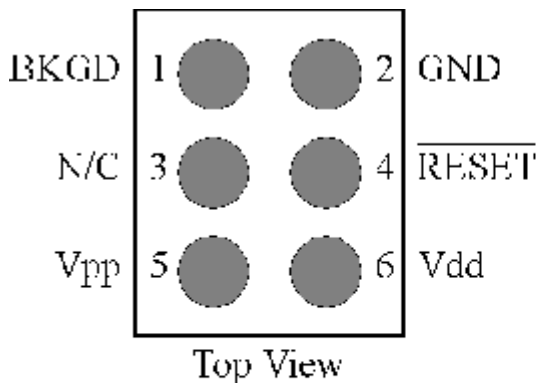
To maximise your 68HC12 debugging performance we recommend that you:-

1. Make your target's MODA and MODB signals available to the BDM hardware. Flex-BDM/68HC12 includes two flying leads for connection to the MODA and MODB signals.
2. Make your target's ECLK signal available to the BDM hardware. Noral's Flex-BDM/68HC12 includes a flying lead for connection to the ECLK signal.

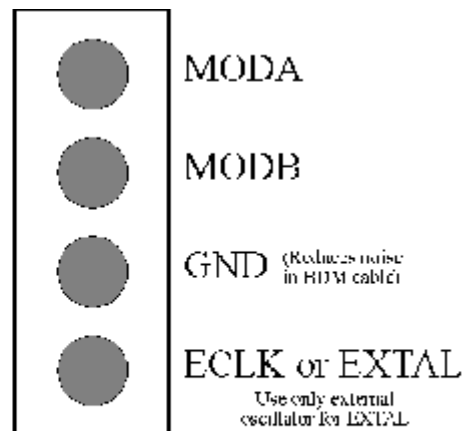
Target Design - Schematics

The diagram below details the pin layout for the standard 6-way 68HC12 BDM connector and shows a typical arrangement for making the additional (optional) signals available via, for example, flying leads from the BDM hardware.

1. A GND signal is shown with ECLK, MODA and MODB to reduce noise in the BDM cable.
2. Synchronous communications can be supported using a CMOS oscillator (Flex-BDM/68HC12 divides the frequency by 2). This design supports dynamic clock switching when it is external to the 68HC12.
3. The four enhanced signals do not need to be on a 0.1" pitch as these are accessed via flying leads. Flex-BDM/68HC12 uses flying leads suitable for connection to 0.025" square posts.

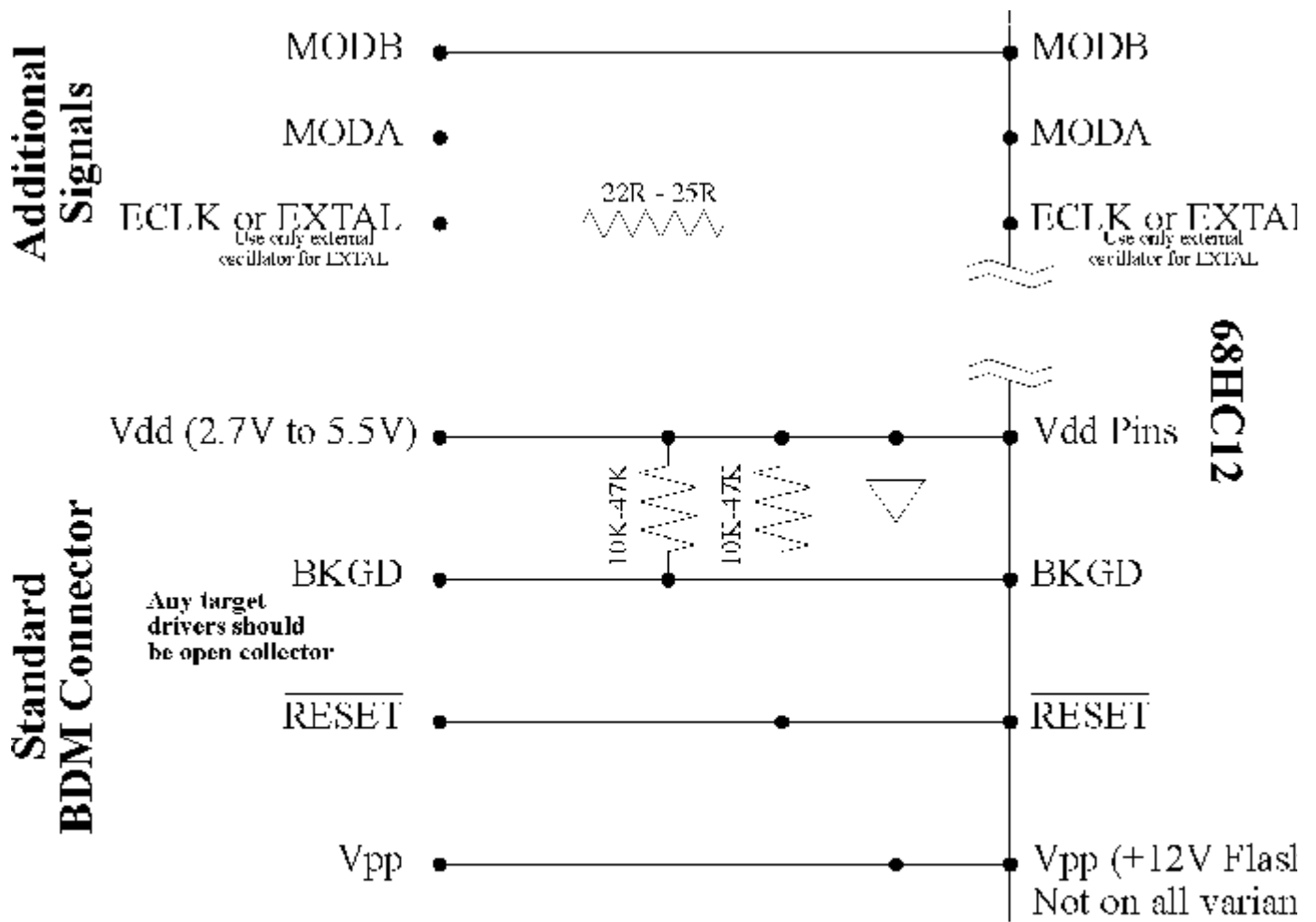


**Standard 68HC12 6-Way
BDM Connector for Target**



**Sample Layout for
Enhanced BDM Signals**

The 68HC12 circuit schematic shown below details the recommended design for the standard 6-way BDM connector plus the additional (optional) ECLK, MODA and MODB signals.



Schematic for Standard BDM Connector with Additional Signals