

# ETec273, Lab #5 – Combinational Design Process

---

Name \_\_\_\_\_

Partner \_\_\_\_\_

## Introduction

In this lab you will complete the combinational design process for the prime number detector used in Lab4. In this lab you will also need to simulate your final design in LogicWorks before coming to class.

## Pre-lab Requirements

All of the pre-lab work is to be done individually. The in-lab work is done with up to one partner.

1. **Paper Design.** In lab4 you found the minimized SOP and POS equations for the prime number detector. In this lab, complete the design process by finding the two functional logic diagrams, the four realizable logic diagrams, and the 'best' schematic. 'Best' in this case is the circuit with the fewest number of IC, the fewest number of gates, then the fastest. Bring you paper design to class.
2. **Simulation.** Enter the 'best' schematic in LogicWorks. Make sure to include all features of a schematic. Using a hex keypad (wo strobe) and a binary probe. Fill out the simulated results in the table below. Once you have the circuit working correctly, print the schematic and bring it to class.

### IMPORTANT!

Use LogicWorks 5 not LogicWorks 3.0.3, which is the icon on the desktop. To run LogicWorks 5, go to the 'Start' menu, then select 'Programs'. LogicWorks 5 does not have the printed page break problems that is such a problem with LogicWorks 3.0.3.

Simulation Truth Table:

$b_3b_2b_1b_0$	PRIME
0 0 0 0	
0 0 0 1	
0 0 1 0	
0 0 1 1	
0 1 0 0	
0 1 0 1	
0 1 1 0	
0 1 1 1	
1 0 0 0	
1 0 0 1	
1 0 1 0	
1 0 1 1	
1 1 0 0	
1 1 0 1	
1 1 1 0	
1 1 1 1	

## In-Lab Requirements

### 1.1 Paperwork Verification

1. Have the instructor or lab assistant check your paperwork before proceeding with the lab.

### 1.2 Construction and Verification

1. Build the circuit from your printed schematic. Verify the output of your circuit in the table below.

$b_3b_2b_1b_0$	PRIME
0 0 0 0	
0 0 0 1	
0 0 1 0	
0 0 1 1	
0 1 0 0	
0 1 0 1	
0 1 1 0	
0 1 1 1	
1 0 0 0	
1 0 0 1	
1 0 1 0	
1 0 1 1	
1 1 0 0	
1 1 0 1	
1 1 1 0	
1 1 1 1	

2. Verify the circuit operation with the instructor or TA.