ETec273, Lab #4 – Combinational Logic Reduction

Name _____

Partner _____

Introduction

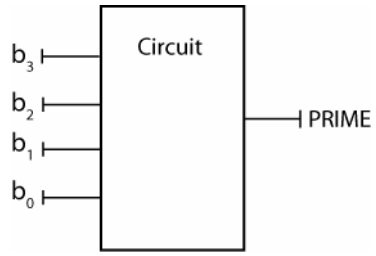
In this lab you will use the reduction techniques covered in class to find the minimum SOP and POS equations. You will then build your circuits and verify that they meet the requirements.

Pre-lab Requirements

1. Know your logic reduction techniques using Karnaugh maps to find the minimum SOP and POS equations.

Design Requirements

Boolean reduction using Karnaugh maps is one step in the combinational logic design process. So, in this lab we will have a design problem. The problem is to design a BCD prime number detector. The prime numbers in this range are 2, 3, 5, and 7. You may use 'don't cares' for non-BCD values. Here is a block diagram for the design, which shows the input signals and output.



1.1 Standard SOP and POS

Show the standard SOP and standard POS equations in shorthand form.

1.2 Reduction Using Karnaugh Maps

1. Find the minimum SOP and POS equations using a Karnaugh maps.

1.2 Construction and Verification

1. Build the circuit for the equation with the fewest number of literals. If they have the same number of literals, pick either one. Verify the output of your circuit in the table below.

$b_3b_2b_1b_0$	PRIME
0 0 0 0	
0 0 0 1	
0 0 1 0	
0 0 1 1	
0 1 0 0	
0 1 0 1	
0 1 1 0	
0 1 1 1	
1 0 0 0	
1 0 0 1	
1 0 1 0	
1 0 1 1	
1 1 0 0	
1 1 0 1	
1 1 1 0	
1 1 1 1	

3. Verify the circuit operation with the instructor or TA.