ETec273, Lab #2 – Logic Devices and Boolean Logic

Name _____

Partner _____

Introduction

In this lab you will be introduced to real fixed logic devices in the 74HCxx family and, using these devices, you will verify some of the Boolean logic principles discussed in class.

Pre-lab Requirements

1. Know your Boolean operators and identities.

2. Understand how gates affect waveforms.

Part One – The DigiDesigner

There are some basic techniques for making use of the DigiDesigner that we should become familiar with so they can be used later.

1.1 Logic Probe

A logic probe is a device that can be connected to a binary signal and indicate the state of the signal. On the DigiDesigner, this is very simple. We just connect a wire long enough to reach anywhere on the DigiDesigner from one of the LED connectors. The LED then indicates the logic level.

1. Connect a long hookup wire to one of the LED connectors. Make the wire long enough to reach the slide switch connectors and anywhere else on the DigiDesigner.

2. Plug the other side into one of the slide switch connectors. Verify that you can change the binary level with the switch and the connected LED indicates the correct level. Use a DMM to measure the voltages when the switch is on and off:

Results:

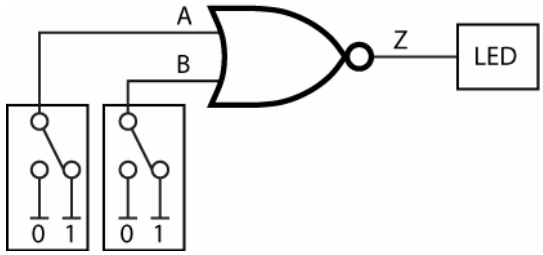
Switch	Measured Voltage	Logic Level (1 or 0)	LED State (On or Off)
ON			
OF			

Comment:

Part Two – The NOR Gate

In this part of the lab, you will connect a 74HC02 to analyze the characteristics of a NOR gate.

1. See the attached data sheet for a 74HC02. Find the pinout, the input voltage thresholds (V_{IH} and V_{IL}), and the propagation delays (t_{PLH} and t_{PHL}). We will use these specs throughout the lab.
2. Connect one of the NOR as follows:



3. Fill in the following truth table and verify, using the switches and LED:

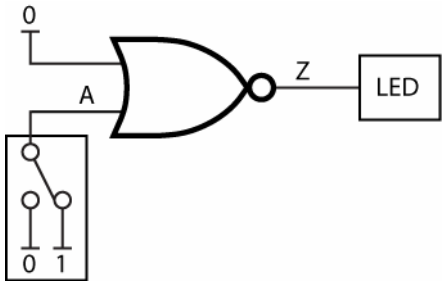
A B	Z	LED (Observed)	A (Voltage)	B (Voltage)
0 0				
0 1				
1 0				
1 1				

4. Discuss the results and compare the Voltages levels with the specified V_{IL} and V_{IH}.

Part Three – The NOR Gate as a NOT

In this part of the lab we will confirm that a NOR can be used as a NOT by connecting one input LOW.

1. Connect a <u>different</u> NOR gate on the 74HC02 as follows:



3. Fill in the following truth table and verify, using the switches and LED:

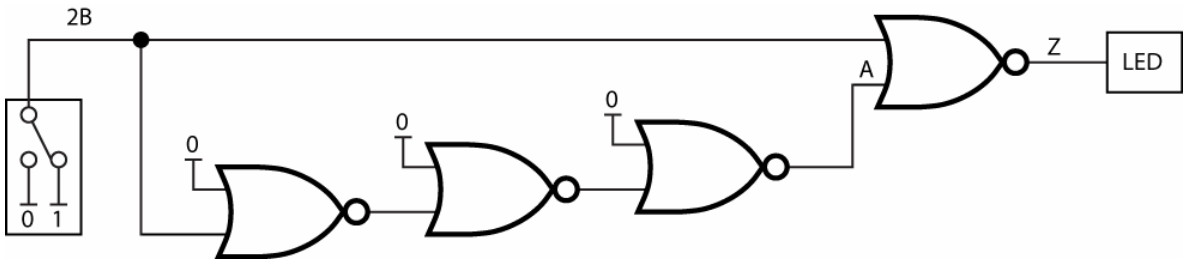
A B	Z	LED (Observed)
0		
1		

4. Comment:

Part Four – '2B or Not 2B' - NOT

In this part of the lab we will learn Shakespeare – NOT – though this circuit is almost as intriguing. We have talked about always showing propagation delays in our waveforms. This circuit illustrates how propagation delays can have an affect on our outputs. The circuit is often referred to as the 2B OR NOT 2B circuit.

1. By modifying the connection from the two previous tests and using two more gates, create the following circuit:

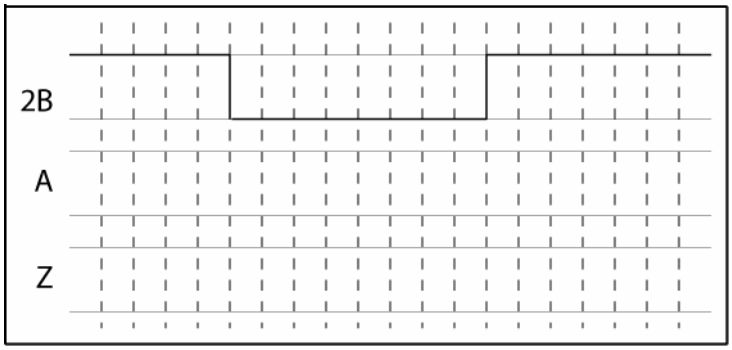


2. Give the simplified Boolean equation for Z

3. Fill out the following truth table:

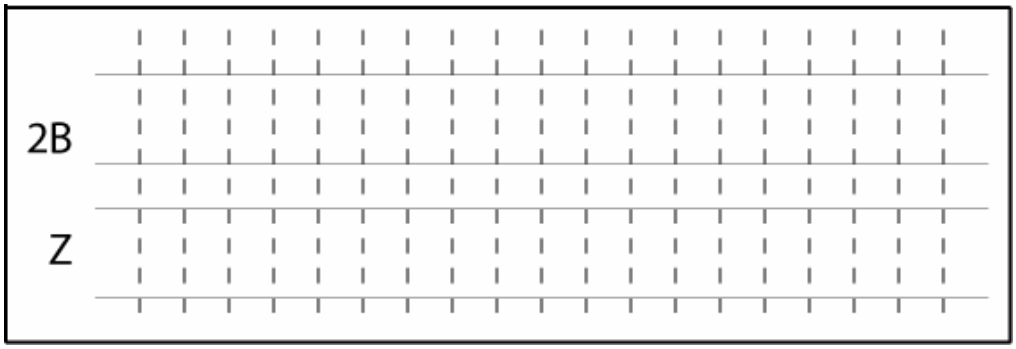
A B	Z	LED (Observed)
0		
1		

4. Sketch your predicted waveform for Z, given the following waveform for 2B



5. Connect the 2B input to the signal generator on the DigiDesigner. Set the frequency to 100kHz. Make sure it is set to a squarewave. Verify the frequency with the oscilloscope.

6. Connect one channel of the oscilloscope to the 2B input and the other to the Z output. Set the trigger and timebase so you can see a glitch on the Z output. Sketch the waveforms below showing the timing relationship between the 2B signal change to the glitch and the width of the glitch.



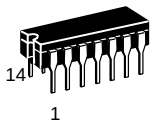
7. Compare these numbers with the propagation delays specifications from the data sheet. Discuss your findings.

MC54/74HC02A

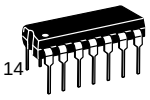
Quad 2-Input NOR Gate
High–Performance Silicon–Gate CMOS

The MC54/74HC02A is identical in pinout to the LS02. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

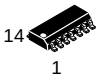
- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 40 FETs or 10 Equivalent Gates



J SUFFIX
CERAMIC PACKAGE
CASE 632–08



N SUFFIX
PLASTIC PACKAGE
CASE 646–06



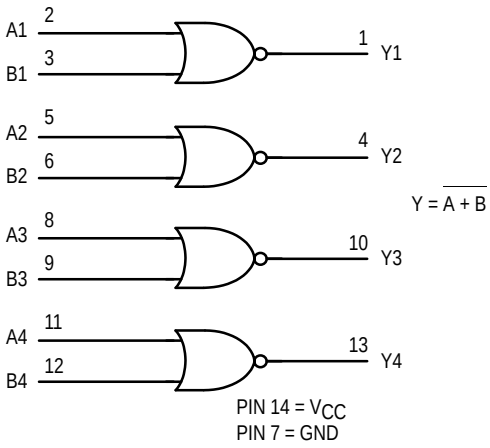
D SUFFIX
SOIC PACKAGE
CASE 751A–03

DT SUFFIX
TSSOP PACKAGE
CASE 948G–01

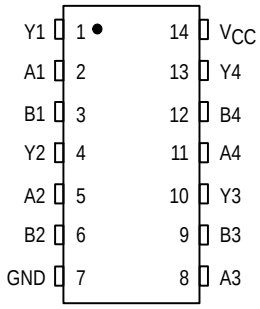
ORDERING INFORMATION

MC54HCXXAJ	Ceramic
MC74HCXXAN	Plastic
MC74HCXXAD	SOIC
MC74HCXXADT	TSSOP

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	H
L	H	L
H	L	L
H	H	L

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, Plastic or Ceramic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package Ceramic DIP	 260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C
Ceramic DIP: – 10 mW/°C from 100° to 125°C
SOIC Package: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V $\|I_{out}\|$ ≤ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\|$ ≤ 2.4 mA $\|I_{out}\|$ ≤ 4.0 mA $\|I_{out}\|$ ≤ 5.2 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.7 5.2	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25°C	≤ 85°C	≤ 125°C	
V_{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 20$ μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		$V_{in} = V_{IH}$ or V_{IL} $\|I_{out}\| \leq 2.4$ mA $\|I_{out}\| \leq 4.0$ mA $\|I_{out}\| \leq 5.2$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $\|I_{out}\| = 0$ μA	6.0	1.0	10	40	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS ($C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			– 55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	2.0 3.0 4.5 6.0	75 30 15 13	95 40 19 16	110 55 22 19	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, $V_{CC} = 5.0$ V	
C_{PD}	Power Dissipation Capacitance (Per Gate)*	22	pF

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

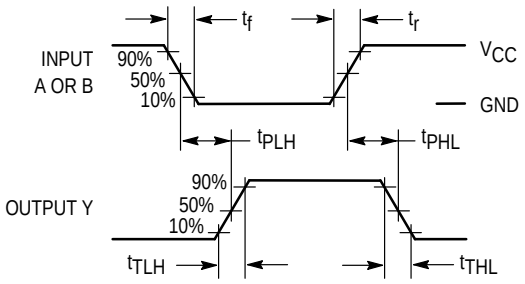
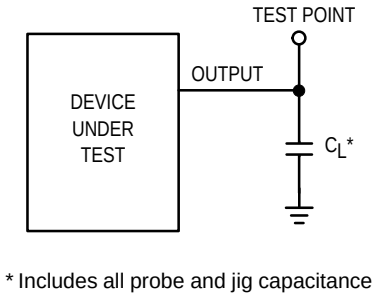


Figure 1. Switching Waveforms



* Includes all probe and jig capacitance

Figure 2. Test Circuit

EXPANDED LOGIC DIAGRAM
(1/4 OF THE DEVICE)